IN THE SPECIFICATION:

Please amend the specification pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked up" version pursuant to 1.121):

Page 3, delete the last paragraph and insert the new last paragraph as follows:

The computer system described herein , and illustrated in Figure 1, is a schematic diagram of the system. In Figure 1, reference numeral 2 denotes a program memory which holds programs in the form of a plurality of instructions. The program memory 2 is connected to an instruction cache 3 which is connected to instruction fetch/decode circuitry 4. The fetch/decode circuitry issues addresses to the program memory and received on each fetch operation a 64 bit instruction from the program memory 2 (or cache 3). Each 64 bit instruction can define two operations or a single operation. The decode unit 4 evaluates the opcode and transmits the appropriate control signals along X and Y channels $5_x,5_y$. Each channel comprises a SIMD execution unit $8_x,8_y$ which includes three data processing units,

Page 5, delete the first full paragraph and insert the new first paragraph as follows:

processing unit. The destination address DST identifies a destination register into which a result of data processing will be placed. The operands and results are conveyed between the register file 10 or 11 and the respective data processing unit via the access paths, 12,14. In the case of load/store operations, the instruction formats allow memory access addresses A_x,A_y to be formulated from data values held in the registers as described in our copending U.S. Patent Application Serial No. 09/935,294 as described later. The load/store units access a common address space in the form of a data memory 16 via a dual ported data cache DCACHE 15. For this purpose, each load/store unit has a 64 bit data bus D_x,D_y and a 64 bit address bus A_x,A_y.

Page 11, delete the last paragraph and insert the new last paragraph as follows:

After comparing the test code specified in the addressed Treg byte with each of the condition codes CCX0 ... CCX7 (assuming the operation is being executed on the X side of the machine), then the specified operation is carried out on the SIMD lanes where there is a match, and is not carried out on the SIMD lanes where there is no match. An example is illustrated in Figure 7. Assumed that the operation illustrated in Figure 6 and described above has been carried out and that condition codes CCX0 to CCX7 have been set as described above depending on the results of the arithmetic operation in each of the SIMD lanes b_0 ...b_7. It is assumed for this example that the condition codes are $_{b0}$ 0010, b_1 0101, b_2 0011, b_3 0010, b_4 0010 b_5 0100. This is illustrated in the condition code register in Figure 7. Let us also assume that the addressed test register byte in the TST field of the instruction holds the condition code 0011. This denotes the condition Carry Set C. SIMD satisfies this condition. Assume that the subsequent operation to be carried out is also an ADD instruction operating on the byte packed contents of two source registers SRC1,SRC2 with the results to be loaded into a destination register DST. Because a test register byte has been specified, the addition operation is only effected on the

IN THE CLAIMS:

Please amend the claims pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked up" version pursuant to 1.121):

Cancel claim 6.